REMARKS

In response to the above-identified Office Action, Applicants amend the application and seek reconsideration thereof. In this response, Applicants amend Claims 20 and 25. Applicants do not add or cancel any claims. Accordingly, Claims 20-29 are pending.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attachment is captioned "Version With Markings To Show Changes Made."

I. Claims Rejected Under 35 U.S.C. § 102(e)

The Patent Office rejects Claims 20-23 and 27-29 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,218,706 to Waggoner, et al. ("Waggoner").

In order to anticipate a claim, the relied upon reference must disclose every limitation of the claim. Amended independent Claim 20 recites forming a performance circuit occupying a first well of an integrated circuit substrate, forming a protection circuit occupying a second well of an integrated circuit substrate separate from the first well, and coupling the protection circuit to the performance circuit. Applicants submit that Waggoner fails to disclose all of these limitations.

In maintaining the rejection, the Patent Office relies on Waggoner to show providing a performance circuit (T1, T2), forming a protection circuit (D3), and coupling the protection circuit to the performance circuit (Figure 8). The Patent Office states further that the performance circuit area (T1 and T2 located between T4 and VSS) and the protection circuit area (D3 located between VDD and R3) are distinct areas such that Waggoner anticipates the rejected claims. In response, Applicants note that amended Claim 20 recites that the performance circuit occupies a first well of an integrated circuit substrate while the protection circuit occupies a second well of an integrated circuit substrate separate from the first well, which is not disclosed by Waggoner.

Placing a performance circuit and the protection circuit in different wells of a substrate insures the best utilization of integrated circuit space. For example, separation of the performance circuit and the protection circuit allows the transistor devices (e.g., performance circuitry) to be scaled independent of the protection circuits (Applicants' specification, page 19, lines 12-15.) Such a partitioning advantageously maximizes the protection circuit current capability and

minimizes the total capacitance of the performance circuit (Applicants' specification, page 10, line 24 through page 11, line 2). Applicants submit that Waggoner fails to disclose any teaching that would lead one skilled in the art to create an integrated circuit substrate having a performance circuit and a protection circuit formed in separate wells of the integrated circuit substrate.

Accordingly, Applicants respectfully request withdrawal of the rejection of amended independent Claim 20. Claims 21-23 and 27-29 depend from independent Claim 20 and are not anticipated at least for the same reasons.

II. Claims Rejected Under 35 U.S.C. §103(a)

The Patent Office rejects Claims 24-26 under 35 U.S.C. 103(a) as being obvious over Waggoner in view of U.S. Patent No. 6,274,908 to Yamaguchi, et al. ("Yamaguchi"). Applicants respectfully traverse this rejection.

In order to render a claim obvious, the relied upon references must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art. Claims 24-26 depend from amended independent Claim 20, which recites forming a performance circuit occupying a first well of an integrated circuit substrate, forming a protection circuit occupying a second well of an integrated circuit substrate separate from the first well, and coupling the protection circuit to the performance circuit. Applicants submit that the cited references in combination fail to teach or suggest all of these limitations.

In maintaining the rejection, the Patent Office acknowledges that Waggoner does not teach performing a plurality of unit diodes as recited in Claims 24-26. The Patent Office relies on Yamaguchi to cure this deficiency. In response, Applicants note that the combination of Waggoner and Yamaguchi fails to teach or suggest an integrated circuit substrate having a performance circuit formed in a first well of the substrate and a protection circuit formed in a second well of the substrate separate from the first well such that the protection circuit and the performance circuit are coupled, as recited in Applicants' amended independent Claim 20, upon which Claims 24-26 are

dependent. Thus, for the reasons outlined above, the cited references in combination fail to teach or suggest all of the limitations of Claims 24-26.

Accordingly, Applicants respectfully request withdrawal of the rejection of Claims 24-26.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 7/25, 2002

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231, on July 25, 2002.

Lillian E. Rodriguez 7-25-02

Lillian E. Rodriguez July 25, 2002

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims as follows:

20. (Amended) A method of forming an integrated circuit comprising:

forming a performance circuit occupying a first [area] well of an integrated circuit substrate;

forming a protection circuit occupying a second [area] well of an integrated circuit substrate separate from the first well [area]; and

coupling the protection circuit to the performance circuit.

25. (Twice Amended) The method of claim [20, a] 24, the doped region being a first doped region of a first dopant in [a] the second well of the substrate, the second well being doped with a first concentration of a second dopant and [a] the junction region separating the first doped region from the second well, wherein forming a protection circuit includes forming a third doped region in the second well adjacent the junction region, the third doped region doped with a second concentration of the second dopant.